

## CLAIMS

What is claimed is:

- 1 1. A frequency synthesizer for generating a data-modulated output signal based on a reference signal  
2 and an input data signal, the frequency synthesizer comprising:
  - 3 (a) a phase-locked loop (PLL) circuit configured to receive the reference signal and generate the  
4 data-modulated output signal;
  - 5 (b) a first data-modulation path configured to (i) generate a first data-modulated input signal based on  
6 the input data signal and (ii) apply the first data-modulated input signal at a voltage-controlled oscillator  
7 (VCO) of the PLL circuit; and
  - 8 (c) a second data-modulation path configured to (i) generate a second data-modulated input signal  
9 based on the input data signal and (ii) apply the second data-modulated input signal at a frequency divider of  
10 the PLL circuit.
- 11 2. The invention of claim 1, wherein the first and second data-modulated input signals have  
12 substantially complementary frequency responses.
- 13 3. The invention of claim 1, wherein:
  - 14 the PLL circuit comprises a phase detector, a loop filter connected to the phase detector, the VCO  
15 connected to the loop filter, and the frequency divider, which is part of a feedback path connecting the VCO  
16 and the phase detector.
- 17 4. The invention of claim 3, wherein:
  - 18 the first data-modulation path has a high-pass frequency response corresponding substantially to a corner  
19 frequency of the loop filter; and
  - 20 the second data-modulation path has a low-pass frequency response corresponding substantially to the  
21 corner frequency of the loop filter.
- 22 5. The invention of claim 3, wherein:
  - 23 the phase detector is configured to generate a phase-difference signal based on the reference signal and a  
24 frequency-divided signal from the frequency divider;
  - 25 the loop filter is configured to generate a loop-filtered signal based on the frequency-divided signal from  
the phase detector;

6 the VCO is configured to generate the data-modulated output signal based on the loop-filtered signal  
7 from the loop filter and the first data-modulated input signal from the first data modulation path; and  
8 the frequency divider is configured to generate the frequency-divided signal based on the data-modulated  
9 output signal from the VCO and the second data-modulated input signal from the second data modulation  
10 path, wherein the second data-modulated input signal determines a division factor applied by the frequency  
11 divider to the data-modulated output signal to generate the frequency-divided signal.

1 6. The invention of claim 1, wherein the second data modulation path comprises a sigma-delta  
2 modulator configured to generate the second data-modulated input signal based on the input data signal.

1 7. The invention of claim 6, wherein frequency synthesizer is configured to operate with two or  
2 more different reference signals and the second data modulation path further comprises:

3 a scaling block configured to adjust gain of the second data modulation path based on a selected reference  
4 signal; and

5 a carrier-selection block configured to inject a carrier frequency based on the selected reference signal.

6 8. The invention of claim 6, wherein the frequency synthesizer applies Gaussian frequency shift  
7 keying (GFSK) data modulation and the input data signal is Gaussian low-pass filtered prior to application to  
8 the first and second data modulation paths.

9 9. The invention of claim 6, wherein the sigma-delta modulator quantizes spurious signals to high  
10 frequencies that are attenuated within the PLL circuit.

1 10. The invention of claim 6, wherein the sigma-delta modulator comprises:

2 (i) an adder; and

3 (ii) a noise-shaping loop, wherein:

4 the adder is configured to generate a summation signal based on the input data signal and an output signal  
5 from the noise-shaping loop, wherein:

6 a set of one or more most significant bits (MSBs) of the summation signal corresponds to the second  
7 data-modulation input signal applied to the frequency divider; and

8 a set of one or more least significant bits (LSBs) of the summation signal is fed back as an input signal to  
9 the noise-shaping loop.

1 11. The invention of claim 10, wherein the sigma-delta modulator functions as a quantizer with  
2 quantization error fed back into the quantizer via the noise-shaping loop.

1        12.     The invention of claim 1, wherein the VCO is an analog VCO, the first data-modulated input  
2 signal is an analog signal, and the first data modulation path comprises a digital-to-analog converter (DAC) to  
3 generate the analog first data-modulated input signal.

TO BE FORWARDED TO THE PATENT OFFICE